GMX™ DMA III

Double Density Floppy Disk Controller

User's Manual

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GIMIX DMA III DOUBLE DENSITY DISK CONTROLLER #68

The GIMIX DMA (Direct Memory Access) DISK CONTROLLER has the capabilities needed to realize the full potential of todays sophisticated multi-user/multi-tasking operating systems such as OS-9 and UniFLEX.

FEATURES

HIGH SPEED using bi-polar logic DMA circuitry for guaranteed operation at 2MHz. DMA transfers take place at full bus speed using 6809 cycle steal DMA. Once the required parameters are passed to the controller and DMA transfer is initiated the processor is free for other tasks. Interrupts can be generated to indicate the completion of the transfer.

SINGLE AND DOUBLE DENSITY data storage on any combination of 5.25" and 8" floppy disk drives; single and double headed, single and double track density, up to 4 drives total.

LOW ERROR RATES are insured by a phase-locked loop data recovery circuit (data separator) and adjustable write precompensation circuitry for drives that require precomp. Separate precomp adjustments are provided for 5.25" and 8" drives.

ADDRESSABLE to any 8 byte boundary in the address space (1M byte when extended address decoding is used). It occupies only 8 bytes of address space.

EXTENDED ADDRESSING control using the SS-50C extended address lines. Control of the extended address lines allows the board to perform DMA transfers to and from any address in the 1M byte address space.

FULLY BUFFERED with separate 5.25" and 8" output buffers and schmidt trigger input buffers for the disk drive signals.

SUPPORTS 3ms. STEP RATES for 5.25" 80 track (96 TPI) drives.

The DMA controller leaves the processor free to perform other tasks once the transfer is initiated, unlike programmed I/O disk controllers which require full time use of the processor during data transfers to and from disk. This is extremely important in a multi-user/ multi-tasking environment as the processor can perform other tasks such as console I/O while a disk transfer is in progress.

Note: The GIMIX DMA III disk controller is an updated version of the original GIMIX DMA controller #68. The DMA III is functionally equivalent to, and can be used as a direct replacement for, the original GIMIX DMA controller without hardware or software modifications.

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JUMPER OPTIONS

The controller has several option jumpers which must be properly set before the board can be used. Several of the options are related to the type of drives being used. In most cases proper jumper settings for several different drives are given. If the drives being used are not listed, the drive manufacturer•s documentation should be consulted to help determine the proper settings. The remaining option jumpers are related to the operating system software and the system hardware configuration. The proper jumper settings for use with GIMIX versions of 6809 FLEX are listed in this manual. For other operating systems consult the software documentation for information on proper settings for these jumpers.

5.25" READY OPTION JUMPER (JA-1)

While most 5.25" drive manufacturers use "standard" pinouts for their drive cables, some drives have non-standard pinouts for features not found on all drives. In particular; MICROPOLIS and BASF drives use pin 6 for the READY output from the drive. MICROPOLIS uses pin 34 for the fourth DRIVE SELECT input. Other drives, such as QUME and the SHUGART SA410/SA460, use pin 34 for READY and pin 6 for the fourth DRIVE SELECT.

Jumper area JA-1 (see sheet 1 of the jumper options drawings), in conjunction with JA-3 (below), reconfigures pins 6 and 34 of the 5.25" drive connector J-1 as required by the drives being used.

When 5.25" drives without a READY output are used this option must be disabled as in Figure D. Figures B and C show the proper jumper settings for several drives that have a READY output.

5.25" HEAD LOAD OPTION (JA-2)

MICROPOLIS drives have a separate HEAD LOAD input on pin 2 of the drive cable. JA-2 (see sheet 1, figure E of the jumper options drawings) should be set according to either figure F or G depending on the drives being used.

5.25" DRIVE SELECT #3 OPTION JUMPER (JA-3)

Most 5.25" drives use pin 6 of the drive cable as the fourth DRIVE SELECT input (drive #3). MICROPOLIS drives use pin 34 for this input. JA-3 (see sheet 1, figure H of the jumper options drawings) should be set according to either figure I or J depending on the drives being used.

DRIVE SELECT OPTION (JA-4)

This option enables the drive select outputs of the controller either: whenever the MOTOR-ON line is active (drive motors are on), or only when the HEAD-LOAD output of the 2797 is active. In the drive select with motor-on position (see sheet 1, figure M of the jumper options drawings) the drive select outputs of the controller are enabled whenever the motors are on. This configuration is preferred when double headed drives are used, as it limits the number of times the heads are loaded and unloaded. In the drive select with head load position (see sheet 1, figure L of the jumper options drawings) the drive select outputs of the controller are only enabled when the HEAD-LOAD output of the 2797 is active. This configuration is preferred when using single headed drives.

SIDE SELECT OPTION JUMPER (JA-5)

This option allows the side select output, for double headed drives, to be controlled by either the side select output of the 2797 or by bit 6 in the boards DMA CONTROL REGISTER. This option is factory jumpered for side select from the DMA CONTROL REGISTER (see sheet 1, figure P of the jumper drawings). This is the standard configuration for GIMIX FLEX, OS-9, and UniFLEX. If special applications require side select from the 2797, a trace must be cut and a solder jumper added to connect the pads per sheet 1, figure O.

5.25" and 8" PRECOMP OPTION JUMPER (JA-6)

Write Precompensation (precomp) is recommended by many drive manufacturers, when their drives are used for double density recording. Some drives require precomp on all tracks; certain 8" and 5.25" 96 TPI (80 track) only require precomp on tracks greater than track #43. JA-6 (see sheet 1, figure T of the jumper options drawings) selects the proper precomp option(s) for the drives being used. Figures U, V, and W show the options for 5.25" drives, figures X and Y for 8" drives. If a combination of 5.25" and 8" drives is used, jumpers should be installed to select the proper option for both sizes. For example: if 5.25" drives that require precomp on all tracks and 8" drives that require precomp are combined, install jumpers as shown in BOTH figures V AND Y. If only one size drive is used, install the appropriate jumper for that size drive. The second jumper should be installed at any of the positions for the unused drive size.

Drive manufacturers specify a certain amount of precomp; usually between 100 and 400 ns. The board has provisions for separately adjusting the amount of precomp for 5.25" and 8" drives. If the controller is purchased as part of a complete disk based system, the precomp is factory adjusted for the drives supplied. If purchased separately, the controller is adjusted to 150 ns. for 5.25" drives and 250 ns. for 8" drives, or to the requirements of the drives being used, if specified when the controller was ordered. The adjustments section explains the procedure for adjusting the board for the required precomp. Consult the manufacturers literature to determine the precomp requirements of the drives being used.

8" MOTOR-ON DELAY OPTION JUMPER (JA-7)

Disk drives normally require a certain amount of delay for the motors to come up to speed after they are started. This delay is provided by a timing circuit on the controller. If 8" drives that do not have motor control (the motors are always running) are used this delay can be eliminated. JA-7 (see sheet 1, figure Q of the jumper options drawings) enables or disables the motor-on delay as required.

If 8" drives without motor control are used position the jumper as shown in figure R. If drives with motor control are used position the jumper as shown in figure S.

5.25" HEAD-LOAD DELAY OPTION JUMPER (JA-8)

Most disk drives have a solenoid that loads and unloads the head(s). These drives require a delay, after the heads are loaded, to allow time for the head(s) to settle. This delay is provided by a timing circuit on the controller. Some 5.25", double headed drives do not have a head load solenoid and the head is loaded as soon as the door is closed. These drives do not require any head load delay.

JA-8 (see sheet 2, figure A, of the jumper options drawings) allows the 5.25" head-load delay to be disabled when drives without head-load solenoids are used, figure B, or enabled for drives with a head-load solenoid, figure C.

Note: JA-17 performs a similar function for 8" drives.

JA-9 NOT USED

SOFTWARE WRITE PROTECT OPTION (JA-10)

JA-10 (see sheet 2, figure D, of the jumper options drawings), in conjunction with bit 4 of the boards DRIVE SELECT REGISTER, allows the disk drives to be write protected under software control. When this option is enabled, figure F, and bit 4 of the DRIVE SELECT REGISTER is set low (0), all drives are write protected and no disk write operations are possible until bit 4 is set high (1). Since all bits in the DRIVE SELECT REGISTER are set low on system power up, bit 4 must be set high (1) after power up to enable disk writes. When this option is disabled, figure E, write protect is controlled only by the write protect signals from the individual drives.

JUMPER AREA (JA-11) is reserved for future use.

BA/BS OPTION JUMPER (JA-12)

DMA transfers to and from the board require a signal from the processor indicating that the bus is available to the controller. This signal is provided by the BUS AVAILABLE (BA) and BUS STATUS (BS) lines of the 6809. JA-12 (see sheet 2, figure J, of the jumper options drawings) is used to select either normal 6809 (BA/BS) , figure K, or BA only, figure L, operation. JA-12 is factory jumpered for 6809 operation, figure K.

DMA OPTION JUMPER (JA-13)

JA-13 (see sheet 2, figure M, of the jumper options drawings) selects either of two DMA methods, HALT or CYCLE STEAL. This jumper is factory programmed for cycle steal DMA per figure O. Halt DMA is not used except for special applications.

SLOW MEMORY OPTION JUMPER (JA-14)

Because of the timing requirements of the 2797, slow memory (MRDY) circuitry is required, at bus speeds above 2 MHz,to stretch the system clock whenever the 2797 is accessed. JA-14 (see sheet 2, figure P, of the jumper options drawings) enables or disables the generation of slow memory cycles as required.

In systems operating at 2 MHz. or slower JA-14 should be jumpered as shown in figure Q (slow memory disabled). For systems operating above 2 MHz. jumper JA-14 as shown in figure R (slow memory enabled).

INTERRUPT OPTION JUMPER (JA-15)

JA-15 (see sheet 2, figure S, of the jumper options drawings) is used to connect the interrupt output (INTRQ) from the 2797 to one of the interrupt lines of the bus. This jumper is factory configured for IRQ interrupts (figure U). Since interrupts can be enabled or disabled under software control (by the interrupt enable bit in the DMA Control Register) this jumper can be left in place for non-interrupt driven applications such as FLEX.

8" MOTOR CONTROL OPTION (JA-16)

JA-16 (see sheet 2, figures W,X, and Y of the jumper options drawings) is used to select the polarity of the motor control output (MOTOR ON) at pin 4 of J2, the 8" disk drive cable connector. For most 8" drives, or for use with the AC motor control circuit in the GIMIX 8" DISK CABINET, the jumper should be installed as shown in figure Y, the NORMAL position. In the NORMAL position, the output goes LOW when the motors are to be turned ON. Some 8" drives, the Tandon half height drives for example, require that the motor control signal go HIGH to turn the motors ON. For use with these drives, the jumper should be installed as shown in figure X.

8" HEAD LOAD DELAY OPTION (JA-17)

Most disk drives have a solenoid that loads and unloads the head(s). These drives require a delay, after the heads are loaded, to allow time for the head(s) to settle. This delay is provided by a timing circuit on the controller. Some 8" drives do not have a head-load solenoid; the head is loaded as soon as the door is closed. These drives do not require any head-load delay.

JA-17 (see sheet 2, figure Z, of the jumper options drawings) allows the 8" head-load delay to be disabled when drives without head-load solenoids are used, figure AA, or enabled for drives with a head-load solenoid, figure BB.

Note: JA-8 performs a similar function for 5.25" drives.

DMA EXTENDED ADDRESS COUNTER OPTION (JA-20)

JA-20 (see sheet 2, figure CC of the jumper options drawings) allows the option of having the extended address output from the board (when enabled by Dip-switch S2-10) increment as part of the DMA source/destination address, or remain fixed. The initial value is determined by the value stored in the lower 4 bits of the DMA Control Register. Enabling this option allows DMA transfers to cross a bank address boundary. For example, with this option enabled and a 4K transfer started at address $F800 on bank $A; after the address counter reached $FFFF the extended address would become $B and the remaining 2K would be transferred to bank $B beginning at address $0000. If this option is disabled, the extended address would remain fixed at $A for the entire transfer. Note: earlier versions of the GIMIX DMA Controller did not have this option; the extended address output did not increment. This option factory enabled (figure DD). For special applications where this feature is not desired, remove the factory jumper and install a jumper per figure EE.

DIP-SWITCH OPTIONS

ADDRESSING OPTIONS (S1 and S2 sections 1 through 8)

The board occupies 8 bytes of address space (4 for the board registers and 4 for the 2797 registers) and can be addressed to any 8 byte boundary in the address space. Extended address decoding (SS-50C) is provided. DIP-switch S1 section 1 (S1-1) enables or disables the extended address decoding for the board.

If S1-1 is OFF (OPEN) extended address decoding is disabled and the board only decodes the 16 regular address lines, A0 through A15. DIP-switch S1 sections 6 through 10 correspond to address lines A3 through A7 respectively. DIP-switch S2 sections 1 through 8 correspond to address lines A8 through A15 respectively. These switches must be set to the desired base address of the board. A switch set ON (CLOSED) corresponds to a 1 (HIGH) on that address line and a switch set OFF (OPEN) corresponds to a 0 (LOW).

If S1-1 is ON (CLOSED) the board decodes all 20 SS-50C address lines, A0 through A19 and, in addition to setting the base address of the board, S1-2 through 5 must be set to the desired extended address. DIP-switch S1 sections 2 through 5 correspond to the extended address lines A16 through A19 respectively. A switch set ON (CLOSED) corresponds to a 1 (HIGH) on that address line. A switch set OFF (OPEN) corresponds to 0 (LOW).

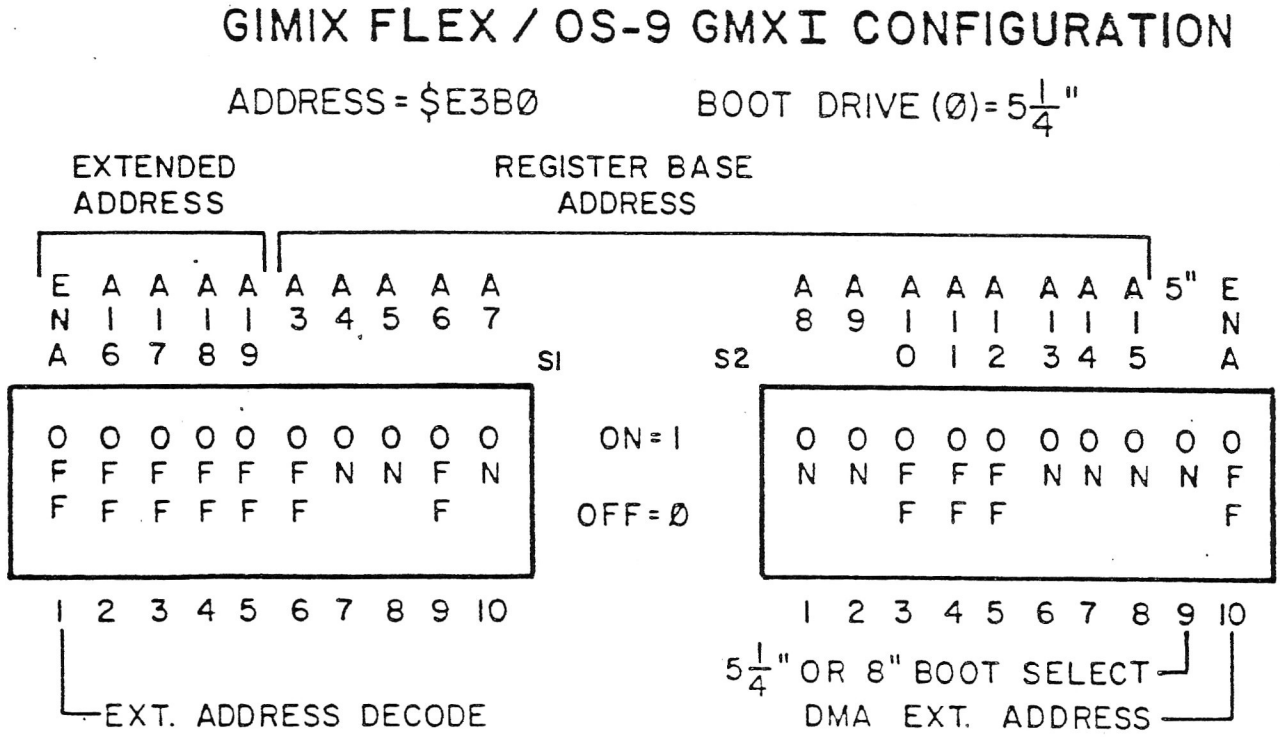


FIGURE 1

OS-9 GMX II & GMX III CONFIGURATION

ADDRESS=$FE3BØ BOOT DRIVE (0)=5 1/4"

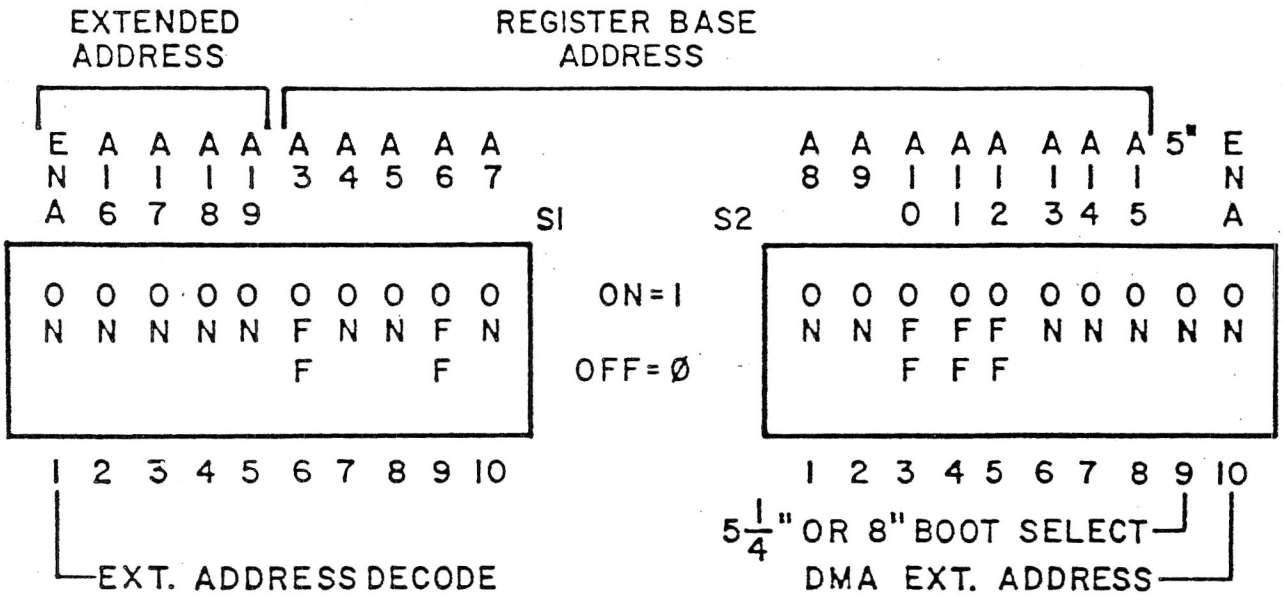


FIGURE 2

UNIFLEX CONFIGURATION

ADDRESS=$FFØØØ

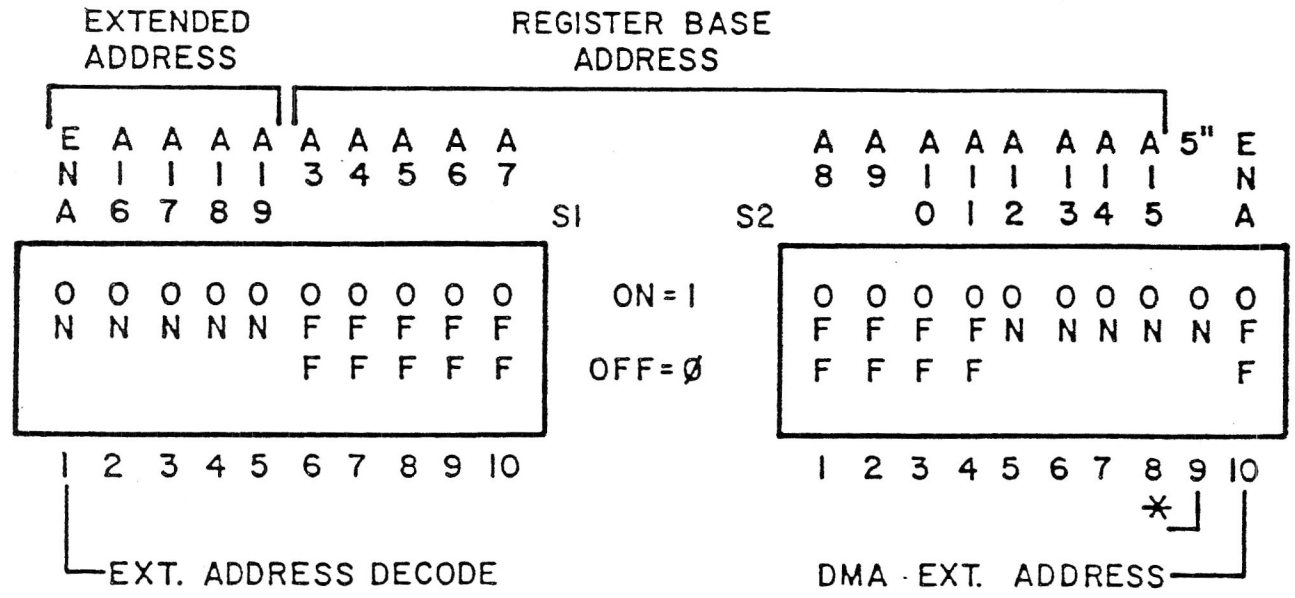


FIGURE 3

* See the UniFLEX documentation for the function of this switch.

5.25" or 8" SENSE SWITCH (S2 section 9)

Bit 0 of the DRIVE SELECT REGISTER is provided to allow the size (5.25" or 8") of the drive installed as drive 0 to be determined by software. The status of this bit is determined by setting S1-9. If drive 0 is a 5.25" drive, S1-9 should be set ON (CLOSED). If drive 0 is an 8" drive, set S1-9 OFF (OPEN). Note: UniFLEX systems may use this switch for other functions. See the UniFLEX documentation for more information.

DMA EXTENDED ADDRESS OPTION (S2 section 10)

The board is capable of driving the SS-50C extended address lines, A16 through A19, during DMA transfers. This allows the board to perform DMA transfers to and from any address in the 1M byte address space of the SS-50C bus. If S2-10 is OFF (OPEN) this option is disabled and the controller only drives the 16 regular address lines A0 through A15. If S2-10 is ON (CLOSED) the controller drives all 20 address lines of the SS-50C bus. The address presented on the 4 extended address lines is determined by the data stored in the lower 4 bits of the DMA CONTROL REGISTER. Bits 0 through 3 of the DMA CONTROL REGISTER correspond to extended address lines A16 through A19 respectively. If the Extended Address Counter Option is enabled by JA-20 (the normal factory configuration) the extended address output will increment after the DMA source/destination address reaches $FFFF, allowing DMA transfers to begin on one bank and continue on the next.

BOARD REGISTERS

The board occupies 8 memory locations and can be addressed to any 8 byte boundary in the 1 megabyte address space. The table below lists the functions of the 8 bytes and assumes the board is at the GIMIX FLEX/OS-9 address, $E3B0.

Base address	$E3B0	Drive Select Register (write) DMA Status Register (read)
	$E3B1	DMA Control Register (write only)
	$E3B2	DMA Starting Address (MSB)
	$E3B3	DMA Starting Address (LSB)
	$E3B4	2797 Command/Status register
	$E3B5	2797 Track Register
	$E3B6	2797 Sector Register
Base address +7	$E3B7	2797 Data Register

The last four are the internal registers of the 2797 floppy disk controller I.C. Information on their functions and programming can be found in the manufacturers data sheets for the 2797.

NOTE: Accessing (read or write) any of the 2797 registers or writing to the DRIVE SELECT REGISTER starts the drive motors.

The first four registers control various functions as described below (addresses in parentheses are for GIMIX FLEX/OS-9).

DRIVE SELECT REGISTER ($E3B0 Write only)

MSB	BIT 7	RESERVED	Reserved for future use.
	BIT 6	CONNECTOR SELECT 0 = 5.25" 1 = 8"	Selects between the 5.25" and 8" drive connectors. Also selects the proper data separator rate and precomp.
	BIT 5	DENSITY SELECT 0 = Double den. 1 = Single den.	Selects between single and double density operation. Selects proper data separator rate and enables precomp for double den.
	BIT 4	WRITE PROTECT 0 = W/protect 1 = W/enable	Write protects all drives when enabled. SOFTWARE WRITE PROTECT OPTION JA-10 must be enabled to use this feature.
	BIT 3	DRIVE SEL. 3	Bits 0 through 3 perform a 1 of 4 drive select function. Any bit set to a 1 selects the associated drive. Only one of the four drives select bits should be a 1 to prevent multiple drives from being selected. 1 = drive selected 0 = drive deselected
	BIT 2	DRIVE SEL. 2	
	BIT 1	DRIVE SEL. 1	
LSB	BIT 0	DRIVE SEL. 0	

Notes: All bits in the DRIVE SELECT REGISTER are cleared to 0 on power up and hardware reset.

Writing to this register will start the drive motors.

DMA STATUS REGISTER ($E3B0 Read only)

MSB	BIT 7	DRQ FLAG	This bit is the same as the DRQ bit in the 2797 status register and the output of the 2797 DRQ signal. See the 2797 data sheet.
	BIT 6	INTRQ FLAG 0 = No INTRQ 1 = INTRQ	Indicates the state of the INTRQ interrupt output from the 2797. This bit is set to a 1 when an interrupt is generated an cleared to 0 when the 2797 status register is read. Active even when bus interrupts are disabled.
	BIT 5	MOTOR DELAY FLAG 0 = Running 1 = Starting	Indicates that the drive motors were stopped then restarted. Used to eliminate software timing when checking for "drives ready".
	BIT 4	DMA ENABLED FLAG 0 = DMA Disabled 1 = DMA Enabled	Indicates that DMA transfers are enabled and an occurence of the 2797 DRQ will cause data to be transferred between the board and memory.
	BIT 3	DMA FAULT FLAG 0 = NO DMA FAULT 1 = DMA FAULT	Indicates that a DMA transfer longer than 16,384 + or - 256 bytes was attempted and the board has stopped the transfer. This can occur because of a hardware fault or if a drive door is opened during a track write (formatting).

NOTE: Data must be written to the DMA STARTING ADDRESS REGISTER (LSB) to reset the DMA FAULT counter and prevent false DMA FAULTS from occuring.

	BIT 2	CONNECTOR SELECT FLAG 0 = 5.25" 1 = 8"	Indicates the drive size, 5.25" or 8", currently selected by the CONNECTOR SELECT bit in the DRIVE SELECT REGISTER.
	BIT 1	RESERVED	Reserved for future use
LSB	BIT 0	SENSE SWITCH FLAG 0 = S2-9 OFF (8") 1 = S2-9 ON (5.25	Indicates the state of the sense switch, S2-9. Used by FLEX and OS-9 to determine what size drive is installed as drive 0.

DMA CONTROL REGISTER ($E3B1 WRITE ONLY)

MSB	BIT 7	INTERRUPT ENABLE 0 = Int. Disable 1 = Int. Enable	Enables the interrupt output from the board to the bus. Interrupt jumper JA-15 must also be set for the desired interrupt line. Allows software switch between interrupt and non-interrupt operation.
	BIT 6	SIDE SELECT 0 = Side Zero 1 = Side One	Used to select between side zero and side one when using double-headed drives. Side select jumper JA-5 must be set for side select from control register in order to use this bit.
	BIT 5	DMA DIRECTION 0 = READ FROM DISK 1 = WRITE TO DISK	Sets the direction for DMA transfers between disk and memory.
	BIT 4	DMA ENABLE 0 = DMA DISABLED 1 = DMA ENABLED	Enables the DMA circuitry for transfers between disk and memory. DMA must be enabled before a read or write data command is issued to the 2797.
	BIT 3	A19	Bits 0 through 3 are used to set the extended (bank) address that will be placed on the bus by the controller during DMA transfers. To use extended addressing during DMA transfers these bits must be set to the desired address and switch S2-10 must be ON (CLOSED).
	BIT 2	A18	
	BIT 1	A17	
LSB	BIT 0	A16	

Notes: All bits in the DMA CONTROL REGISTER are cleared to 0 on power up and hardware reset.

DMA STARTING ADDRESS REGISTERS ($E3B2 and $E3B3 WRITE ONLY)

The source/destination address for a DMA transfer must be written to the DMA STARTING ADDRESS REGISTERS before a transfer is initiated by issuing a read or write command to the 2797. After each byte is transferred the address is automatically incremented and another byte is transferred, until the 2797 read or write operation is complete. The most significant byte of the 16 bit address is stored in the MSB register ($E3B2) and the least significant byte in the LSB register ($E3B3). If extended addressing (20 bit) is used, the extended address is written to the DMA CONTROL REGISTER bits 0 through 3 (see above). If the source/destination address counters reach $FFFF, the next count will cause the extended address to increment (unless this option is disabled, see JA-20), permitting DMA transfers to cross bank boundaries.

Writing to the DMA STARTING ADDRESS REGISTER (LSB) resets the DMA FAULT counter. This register must be rewritten before every DMA transfer to prevent a false DMA FAULT from occuring.

PROGRAMMING FOR THE GIMIX DMA CONTROLLER

This section is included as a guide to the features of the board, for the user who wishes to write his own operating system or adapt the board to an existing operating system. Information on programming the 2797 can be found in the manufacturers literature.

DRIVE SELECT REGISTER (WRITE)

The functions of the DRIVE SELECT REGISTER bits are described in the preceding section. On power up or after a system reset the following conditions exist: 5.25" drives, double density, and write protect of all drives is selected. All drives are deselected. Before a disk transfer is initiated the drive size, density, and write protect should be set as required and one of the drives selected by setting the appropriate drive select bit to a "1".

DRIVE SELECT REGISTER (READ)

Reading the DRIVE SELECT REGISTER indicates the status of various functions of the board. The basic functions of the flags are described in the preceding section. More detailed information on those that have special significance is given below.

BIT 7: The DRQ FLAG is not normally used for DMA transfers, it is only required if the board is used as a programmed I/O controller.

BIT 6: In an interrupt driven system, the IRQ FLAG can be read to determine whether or not an interrupt was generated by the controller. This bit should also be used, instead of the busy bit in the 2797 status register, to determine when a command has been completed. This eliminates the need for a delay loop that makes the software dependent on system clock speed. The 2797 status register must be read to clear the IRQ FLAG.

BIT 5: The MOTOR DELAY FLAG can be used in routines that check for "drives ready". Normally these routines include a delay loop to insure that a "drives not ready" condition is not caused because the drive motors are not yet up to speed. The MOTOR DELAY FLAG can be used to eliminate delay loops under certain conditions.

Note: The MOTOR DELAY FLAG should not be used when the software may be used with drives that automatically start their motors when they are selected instead of using the MOTOR ON signal from the controller. General purpose software should use appropriate timing loops to allow for motor startup delays.

To use the MOTOR DELAY FLAG, first check the "drives ready" status from the 2797. If this indicates that the drives are ready, normal operation can proceed. If the drives are not ready, the MOTOR DELAY FLAG should be checked. If the MOTOR DELAY FLAG is LOW (0), the motors are at speed and the "drives not ready" can be considered valid and proper action taken to handle the error. If the MOTOR DELAY FLAG is HIGH (1), it should be rechecked until it goes LOW (0). The HIGH to LOW transition indicates that the drive motors have been on long enough to come up to speed. The "drives ready" status from the 2797 should again be checked and if it still indicates "drives not ready" the condition can be considered valid (no disk in the selected drive, door open, etc.) and proper action taken to handle the error. If it indicates that the drives are ready, normal operation can proceed.

BIT 3: Because the 2797 track read and track write commands read or write data continuously, starting when one index pulse is received from the drive and ending on the next, it is possible for control of a transfer to be lost because of a hardware failure or because the drive door is opened during a track write. If this were to occur the board would cycle continuously through the entire address range reading from memory. This runaway condition is prevented by a counter which limits the maximum transfer to 16,384 + or - 256 bytes. If the maximum count is reached the transfer is halted and the DMA FAULT FLAG is set HIGH (1) to indicate a DMA FAULT. The DMA FAULT FLAG should be checked at the completion of any 2797 track write commands to determine if a DMA FAULT has occurred. The DMA FAULT COUNTER is reset by writing to the DMA STARTING ADDRESS REGISTER (LSB). Data must be written to this register before each DMA transfer to reset the counter and prevent false DMA FAULTS.

DMA CONTROL REGISTER

The functions of the DMA CONTROL REGISTER are described in the preceding section. More detailed information for some of the bits is given below. On power up or after a system reset all bits are cleared to 0; interrupts are disabled, side 0 and read are selected, DMA is disabled, the extended address is set to $0.

BIT 7: This bit enables and disables the interrupt output from the board to the bus. It does not affect the interrupt flags in the DRIVE SELECT REGISTER. In an interrupt driven system, this bit must be set by the software to enable bus interrupts. The desired interrupt must also be enabled by the interrupt jumper JA-15. This option allows switching between interrupt and non-interrupt driven software without reconfiguring the board.

BIT 4: DMA must be enabled by setting this bit HIGH (1) before DMA transfers can take place. It must be set before a read or write command is issued to the 2797 or data will be lost.

DMA STARTING ADDRESS REGISTERS (MSB and LSB)

The source or destination address for a DMA transfer must be written to these registers before the transfer is initiated. Once the transfer is started the board increments this address each time a byte is transferred. At the completion of a transfer the DMA STARTING ADDRESS REGISTERS point to the address after the address of the last byte transferred. If the Extended Address Counter Option (JA-20) is enabled and the address increments past $FFFF the extended address will also be incremented by one. It is not necessary to write a new value to the MSB register if a second transfer is to be made, continuing from this address. The LSB register should be re-written, before each transfer or before 16,128 (16K-256) bytes have been transferred, to reset the DMA FAULT counter. IF THE DMA FAULT COUNTER IS NOT RESET BEFORE MORE THAN 16,128 BYTES ARE TRANSFERRED A FALSE DMA FAULT WILL OCCUR, HALTING DMA TRANSFER.

HEAD LOAD DELAY

The board has two separate delay circuits, one for 5.25" drives and another for 8". The proper circuit is selected by the CONNECTOR SELECT BIT. These delays are used to provide the required settling time, after the heads have been loaded. The delay starts whenever the head load output from the 2797 (HLD) becomes active (HIGH). After the delay, the head load timing input to the 2797 (HLT) is made high indicating to the 2797 that the heads are loaded and have had time to settle. The HLT input is also controlled by another delay circuit that provides a delay for the drive motors to come up to speed. Both the HEAD LOAD DELAY and the MOTOR-ON delay must be completed before the HLD input is made HIGH.

Once the HLD output is made active (HIGH), by issuing a command to the 2797 that loads the heads, it does not become inactive (LOW) again until it is specifically reset by issuing a command that unloads the heads or until 15 revolutions of the disk have occurred since the 2797 completed its last command.

To insure proper operation of the HEAD LOAD DELAY circuit and reliable operation of the controller, the HLD output should be made inactive by issuing a command to unload the head each time a different drive is selected. Issuing a head load command will then restart the HEAD LOAD DELAY and allow the proper head settling time.

ADJUSTMENTS

***** CAUTION *****

The GIMIX DMA III is completely calibrated at the factory and should not require recalibration unless the WD 2797 or the components in the adjustment circuits are replaced. Calibration of the board requires care and the proper test equipment. Before attempting to calibrate the board be sure that recalibration is really necessary. Improper recalibration can seriously degrade the performance of the board. The minimum equipment required for calibration is an oscilloscope with an ACCURATE time base and a non-metallic adjustment tool for the trimmer capacitor (C-31). An ACCURATE frequency counter is also helpful but not absolutely necessary.

A total of 5 adjustments are required to completely calibrate the DMA III for both 5" and 8" disks. Following is a list of the step required to calibrate the board. The board should be installed in a functioning system with a monitor program, such as GMXBUG-09, that can be used to store the required values in the boards control registers. JA-18 provides convenient access to the test points required (see fig. 2).

The first four adjustments require monitoring the proper test point, with the oscilloscope set to trigger on the positive-going edge of the signal, and adjusting one of the four trimmer resistors (see fig. 2) for the required positive-going pulse width. The fifth adjustment requires monitoring a test point and adjusting trimmer capacitor C-31 (use a non-metallic adjusting tool) for the correct frequency.

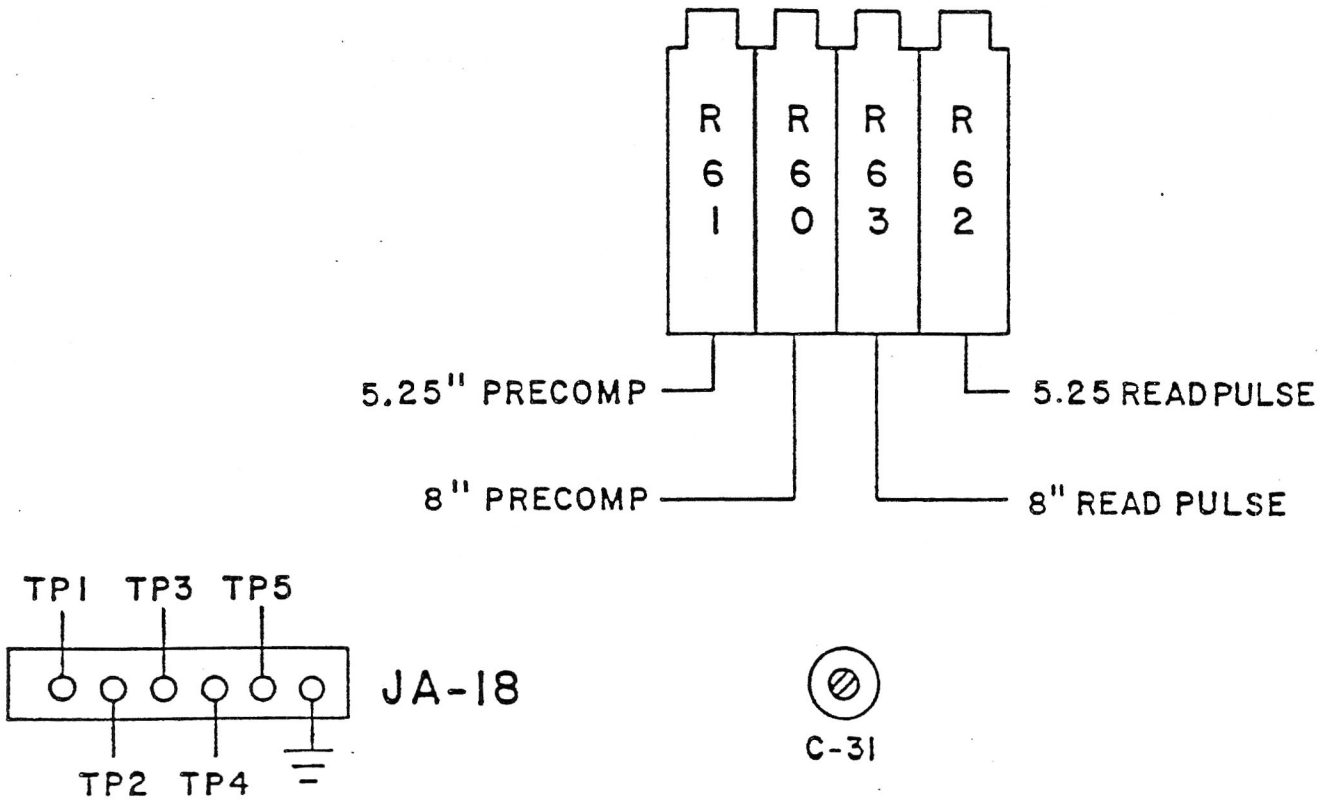


FIGURE 4

STEP	ACTION	RESULT
1:	Power-up system	
2:	Monitor TP-1	4 MHz ±0.5% square wave (1)
3:	Ground TP-5	2797 in adjustment mode
4:	Monitor TP-4	5" Precomp adjustment
	Adjust R-61	150 ns. pulse at TP-4 (2)
5:	Monitor TP-2	5" read pulse width adj.
	Adjust R-62	500 ns. pulse at TP-2
6:	Write $40 at $E3B0	Select 8" drive size (3)
7:	Monitor TP-4	8" Precomp adjustment
	Adjust R-60	250 ns. pulse at TP-4 (2)
8:	Monitor TP-2	8" read pulse width adj.
	Adjust R-63	250 ns. pulse at TP-2
9:	Monitor TP-3	Data Separator clock adj.
	Adjust C-31	500 KHz. sq. wave at TP-3
10:	Un-ground TP-5	Restore 2797 to normal mode

(1): If the 4 MHz. clock is not present, the crystal oscillator circuit is defective; no further adjustments are possible until the problem is corrected.

(2): These are standard precomp settings used by GIMIX, other values can be set by making the pulse width equal the desired precomp.

(3): Assuming that the board is set to the standard base address for FLEX/OS-9 ($E3B0). Use first board address if the board is set to a different address.

Note: Calibration requires a jumper connecting test point TP-5 to ground (the pin to the right of TP-5 on JA-18). The system should NOT be reset while this jumper is installed (TP-5 grounded). This causes the 2797 to enter a special state that prevents calibration or normal operation. If the system is inadvertently reset while TP-5 is grounded, reset the system with the jumper removed to restore the 2797 to its normal state.

DISK DRIVE CONFIGURATION

DRIVE CONNECTIONS

Standard 34 pin (J1) and 50 pin (J2) connectors are provided for the 5.25" and 8" drive cables respectively. The proper connector is selected automatically when the controller is switched between 5.25" and 8" drives using the CONNECTOR SELECT bit in the DRIVE SELECT REGISTER. The length of the cables between the controller and the drives should be kept to a minimum to reduce noise pickup. Ten feet should be considered an absolute maximum for the combined length of both cables.

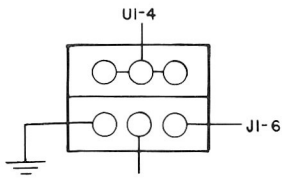
DRIVE PROGRAMMING

Any combination of 5.25" and 8" drives, up to four drives total, can be connected to the controller. The drives themselves must be programmed to respond to the desired drive number (drive select 0, 1, 2, or 3). See the drive manufacturers documentation for information on programming specific drives. If only one size drive is used the drives should be programmed in sequence starting with drive 0. If both 5.25" and 8" drives are used they can be arranged in any desired order starting with drive 0. For example: if two 5.25" and two 8" drives are used, the 5.25" drives could be programmed as drives 0 and 1, the 8" drives would then be 2 and 3, If the 8" drives were programmed as drives 0 and 1, the 5.25" would then be programmed as 2 and 3. They could also be arranged so that drives 0 and 2 are 8" and drives 1 and 3 are 5.25" etc. Regardless of the order chosen, the 5.25" or 8" SENSE SWITCH (S2 section 9) must be set to match the size of the drive programmed as drive 0.

DRIVE TERMINATION

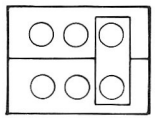
In order for the controller to function properly, the drive cables must be properly terminated. Terminating resistors are provided on the disk drives to terminate the cables. When more than one drive is connected to a single cable the terminating resistors on all drives EXCEPT the last one on that cable (the drive farthest from the controller) must have their terminating resistors removed or disabled. Only the last drive on the cable should have a terminator. If both 5.25" and 8" drives are used the last drive on both cables must have a terminator. Consult the drive manufacturers documentation for information on removing or disabling the terminators.

JA 1



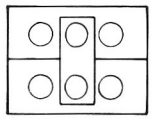
5" READY OPTIONS

FIG. A



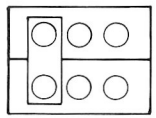
READY FROM PIN 6
MICROPOLIS

FIG. B



READY FROM PIN 34
QUME, SA410/SA460
ETC.

FIG. C



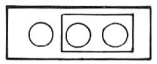
READY DISABLED

FIG. D

JA 2

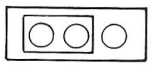
5" HEAD LOAD

FIG. E



HEAD LOAD ENABLED
MICROPOLIS

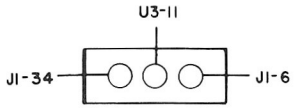
FIG. F



HEAD LOAD DISABLED

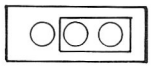
FIG. G

JA3



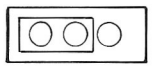
5" DRIVE SELECT
#3 OPTION

FIG. H



NORMAL FOR MOST
DRIVES SHUGART,
MPI, SIEMENS, ETC.

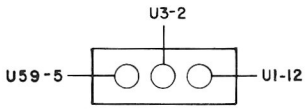
FIG. I



MICROPOLIS

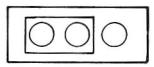
FIG. J

JA 4



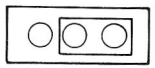
DRIVE SELECT OPTION

FIG. K



DRIVE SELECT WITH
HEAD LOAD

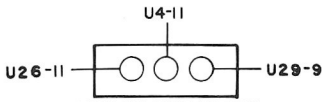
FIG. L



DRIVE SELECT WITH
MOTOR ON

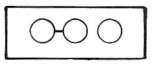
FIG. M

JA5



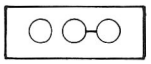
SIDE SELECT OPTION

FIG. N



SIDE SELECT USING
1797 OUTPUT

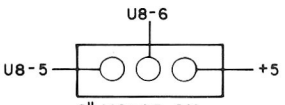
FIG. O



SIDE SELECT USING
CONTROL REGISTER

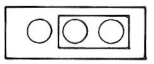
FIG. P

JA 7



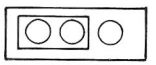
8" MOTOR ON
DELAY OPTION

FIG. Q



NO MOTOR-ON DELAY
(DRIVE MOTORS ALWAYS
ON)

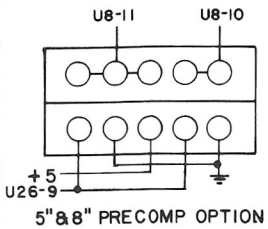
FIG. R



MOTOR-ON DELAY

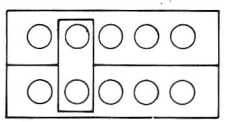
FIG. S

JA 6



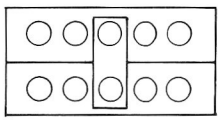
5"&8" PRECOMP OPTION

FIG. T



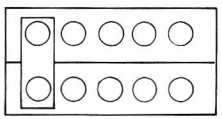
5" PRECOMP DISABLED

FIG. U



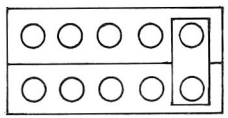
5" PRECOMP ON ALL TRACKS

FIG. V



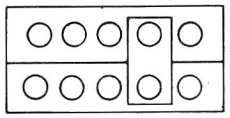
5" PRECOMP ABOVE TRACK
43 (80 TRACK DRIVES)

FIG. W



8" PRECOMP DISABLED

FIG. X

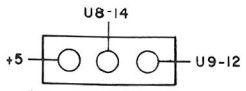


8" PRECOMP ENABLE
ABOVE TRACK 43

FIG. Y

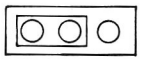
GIMIX INC. 1337 W. 37th PLACE, CHICAGO, IL. 60609	
2-7-83	
GMX™ DMA III	
JUMPER OPTIONS SHEET 1	C24-0074-1

JA 8



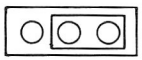
5" HEAD LOAD DELAY TIME OPTION

FIG. A



HEAD LOAD DELAY DISABLED (DRIVES WITHOUT HEAD LOAD SOLENOID)

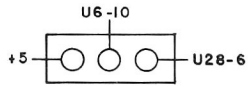
FIG. B



75ms. HEAD LOAD DELAY ENABLED

FIG. C

JA 10



SOFTWARE WRITE PROTECT OPTION

FIG. D

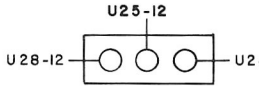
SOFTWARE WRITE PROTECT DISABLED

FIG. E

SOFTWARE WRITE PROTECT ENABLED

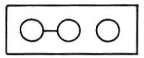
FIG. F

JA 11



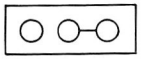
RESERVED FOR FUTURE USE

FIG. G



RESERVED

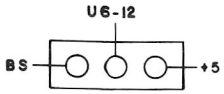
FIG. H



NORMAL

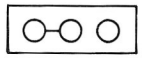
FIG. I

JA 12



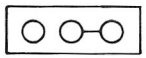
6809 BA/BS OPTION

FIG. J



6809 (NORMAL)

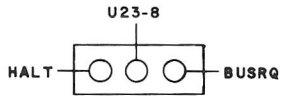
FIG. K



NO BS

FIG. L

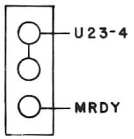
JA 13



DMA OPTION

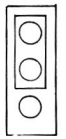
FIG. M

JA 14



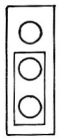
SLOW MEMORY

FIG. P



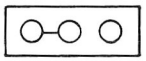
DISABLED

FIG. Q



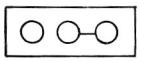
ENABLED

FIG. R



HALT

FIG. N



CYCLE STEAL

FIG. O

JA 15

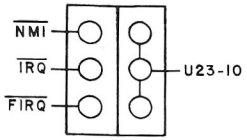
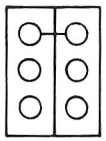
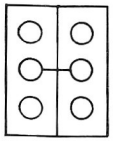


FIG. S



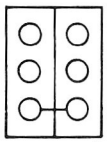
NMI ENABLED

FIG. T



IRQ ENABLED

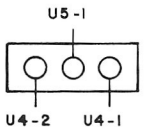
FIG. U



FIRQ ENABLED

FIG. V

JA 16

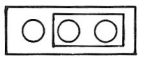


8" MOTOR CONTROL

FIG. W

INVERTED

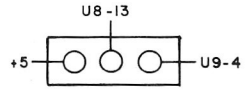
FIG. X



NORMAL

FIG. Y

JA 17



8" HEAD LOAD DELAY OPTION

FIG. Z

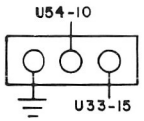
HEAD LOAD DELAY DISABLED (DRIVES WITHOUT HEAD LOAD SOLENOID)

FIG. A A

60ms. HEAD LOAD DELAY ENABLE

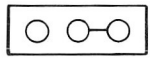
FIG. BB

JA 20



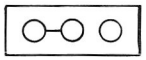
EXT. ADDRESS COUNTER OPTION

FIG. CC



ENABLED

FIG. DD



DISABLED

FIG. EE

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2-10-83 Clark		
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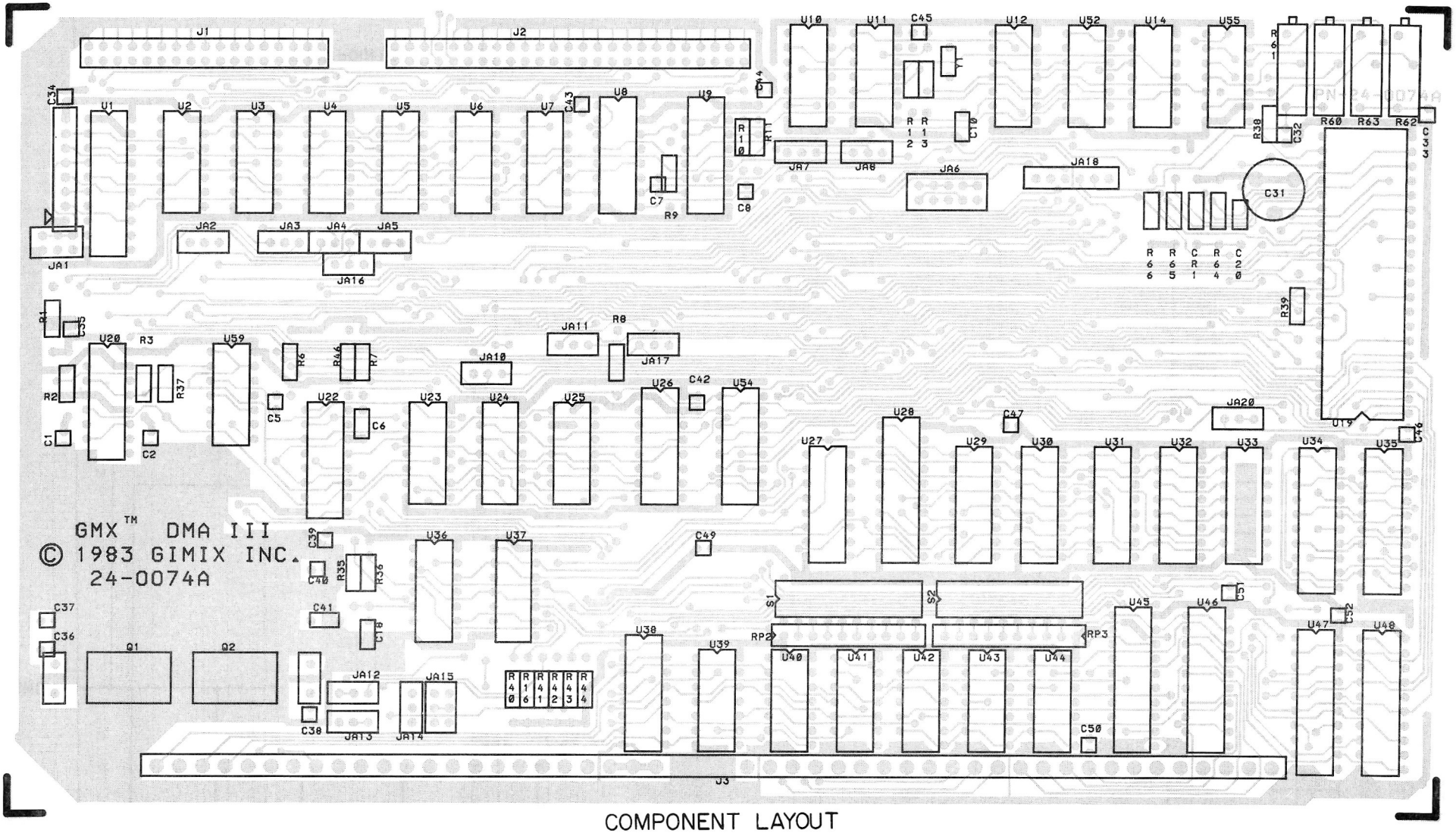
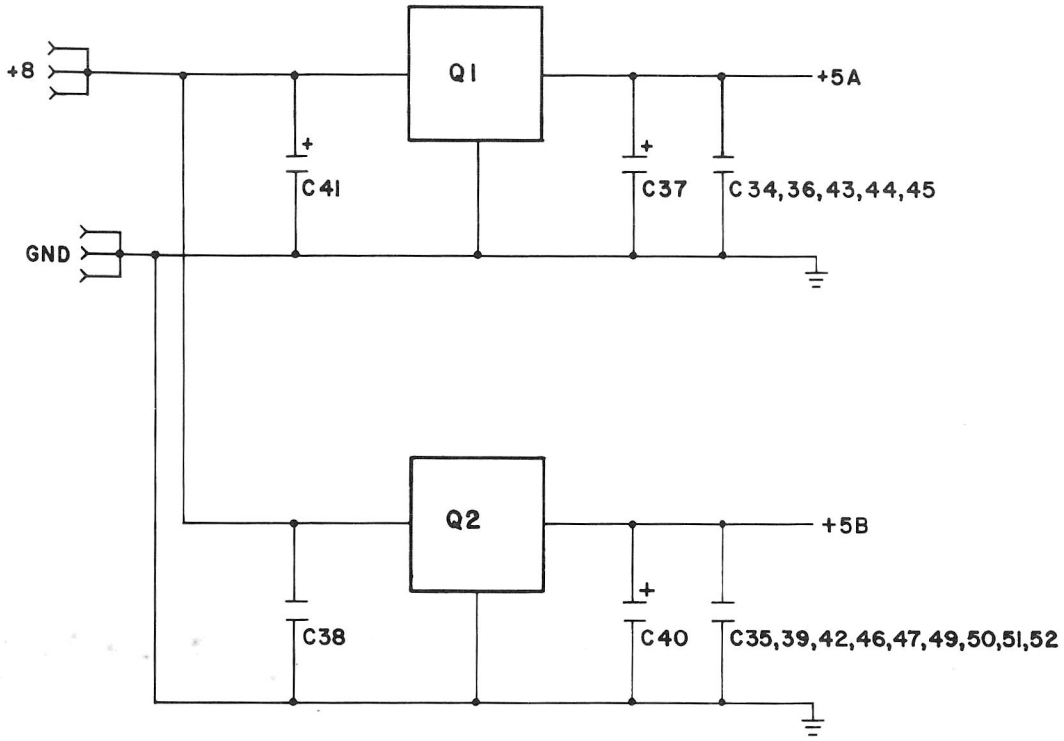
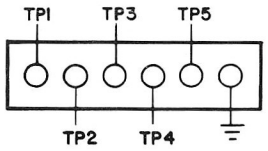
JUMPER OPTIONS SHEET 2		C24-0074-2



COMPONENT LAYOUT

POWER & GROUND PINOUTS





JA18
TEST POINTS

IC.NO.	+5A	+5B	GND.
U1	20		10
U2	14		7
U3	14		7
U4	14		7
U5	14		7
U6	14		7
U7	14		7
U8	16		8
U9	16		8
U10	14		7
U11	14		7
U12	14		7
U14	14		7
U19	21		20
U20		16	8
U22		16	8
U23		14	7
U24		14	7
U25		14	7
U26		16	8
U27		16	8
U28		20	10
U29		16	8
U30		16	8
U31		16	8
U32		16	8
U33		16	8
U34		20	10
U35		20	10
U36		14	7
U37		14	7
U38		16	8
U39		14	7
U40		14	7
U41		14	7
U42		14	7
U43		14	7
U44		14	7
U45		20	10
U46		20	10
U47		20	10
U48		20	10
U52	14		7
U54		16	8
U55	14		7
U55		14	7

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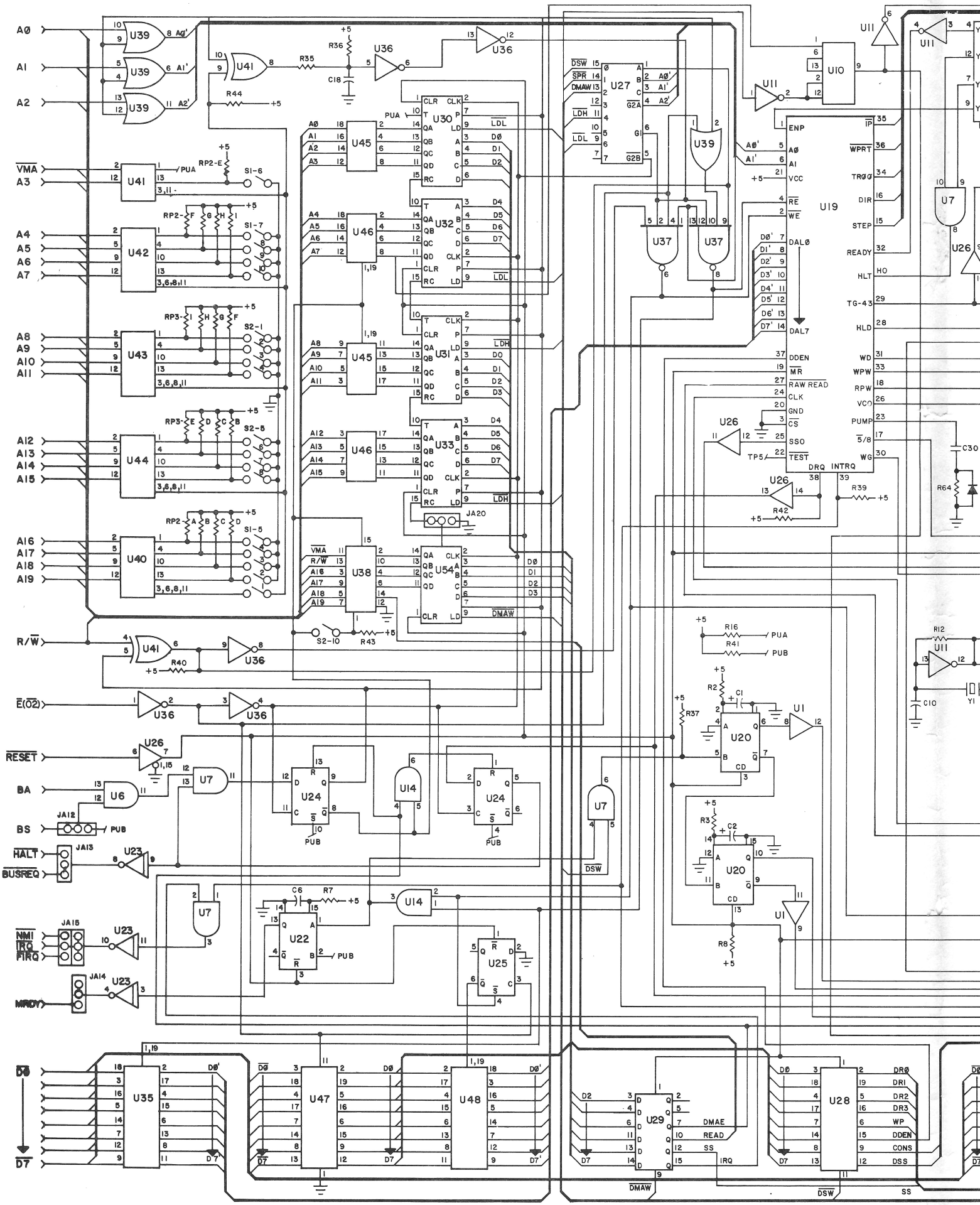
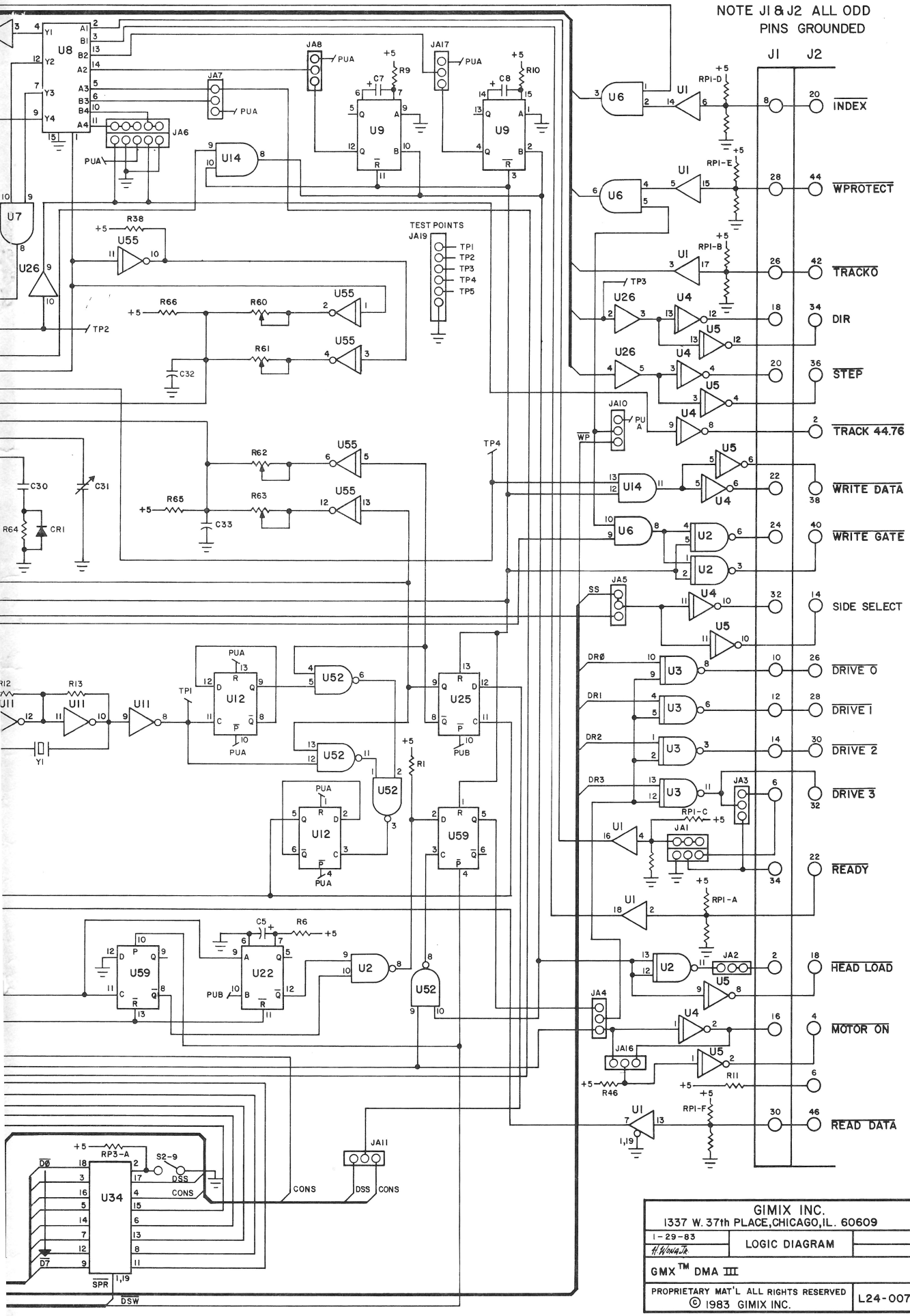
2-14-83	LOGIC SUPPLY	Chuck
GMX™ DMA III		
		L24-0074A-2


A0
A1
A2
VMA
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
R/W
E(02)
RESET
BA
BS
HALT
BUSREQ
NMI
IRQ
FIRQ
MRDY
D0
D7
U39
U41
U36
U45
U46
U30
U31
U32
U33
U42
U43
U44
U40
U38
U54
U27
U10
U11
U19
U26
U37
U7
U6
U23
U24
U14
U22
U25
U20
U1
U35
U47
U48
U29
U28
R36
R35
R44
C18
RP2-E
RP2-F
RP2-G
RP2-H
RP3-H
RP3-G
RP3-F
RP3-E
RP3-D
RP3-C
RP3-B
RP2-A
RP2-B
RP2-C
RP2-D
SI-6
SI-7
SI-1
SI-5
S2-1
S2-5
S2-10
R40
R43
JA20
JA12
JA13
JA15
JA14
PUA
PUB
DSW
DMAW
LDL
LDH
DALØ
DAL7
DRQ
INTRQ
TP5
R39
R42
C30
R64
R16
R41
R12
C10
Y1
R2
C1
R37
R3
C2
R8
C6
R7
DMAE
READ
SS
IRQ
DRØ
DR1
DR2
DR3
WP
DDEN
CONS
DSS



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1-29-83 H. Howard Jr.	LOGIC DIAGRAM
GMX™ DMA III	
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